VLSI Systems Design

Iain McNally

< 12 lectures - Tuesday Afternoons\(^1\)

12 lab sessions - **Every** Thursday Morning

+ occasional extra lab sessions?

\(^1\)lectures advertised via the course e-mail list
VLSI Systems Design

- Content

  - Layout for VLSI
    Cell layout, Standard cell layout, Full and semi-custom design,
    Floorplanning, Bit slice design.

  - Digital design using SystemVerilog
    Introduction to SystemVerilog, Design for Synthesis.

  - CAD Tools & Techniques
    Magic VLSI layout editor, HSpice analogue circuit simulator,
    SystemVerilog Hardware Description Language and digital sim-
    ulator, Cadence IC design toolset.
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- **Assessment - 100% Coursework**
  - *Desex1* 10%  Design and optimization of a CMOS gate using Magic
    Mini design exercise (automatically marked?) – No formal write-up
  - *Desex2* 20%  Design of a digital system using SystemVerilog HDL
    Mini design exercise – No formal write-up
  - *Desex3* 35%  Design of a standard cell library using Magic
    Team exercise – Formal report
  - *Desex4* 35%  Bitslice Design using Magic and SystemVerilog HDL
    Individual exercise – Basic documentation (just design diagrams)

- **Assess** 25%  Ongoing laboratory assessment
  Attendance + Progress + Up to date log book

\[
Mark = (Desex1 + Desex2 + Desex3 + Desex4) \times \frac{75 + Assess}{100}
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• Book
  – Integrated Circuit Design
    a.k.a. Principles of CMOS VLSI Design - A Circuits and Systems Perspective
    Neil Weste & David Harris
    Pearson 2011

• Notes & Resources
  – Lecture notes and Design Exercises
    http://secure.ecs.soton.ac.uk/module/ELEC6230/
  – Lab Sheets and Reference Material
    http://secure.ecs.soton.ac.uk/notes/bim/notes/cad/