ELEC3207
Nanoelectronic Devices
“Scientists study the world as it is; engineers create the world that has never been.”

-Theodore von Karman
Engineer
Recommended textbook

- Fundamentals of Modern VLSI Devices
  Y. Taur & T. H. Ning

We will cover some of these chapters.
n-channel MOS Field-Effect-Transistor

- **Gate (Metal)**
- **SiO$_2$ (Oxide)**
- **Source n$^+$**
- **Drain n$^+$**
- **p-type Si (Semiconductor)**

nMOS uses electrons for a channel.
p-channel MOS Field-Effect-Transistor

Gate (Metal)

SiO$_2$ (Oxide)

p-channel (hole) inversion layer

Source p$^+$

n-type Si (Semiconductor)

Drain p$^+$

pMOS uses holes for a channel.
Oxide thickness is extremely thin ≈ 1.0 nm.

We use both nMOS and pMOS for LSI circuits.

Complementary MOS (CMOS) circuits
SiN tensile film

SiO$_2$ offset spacer

SiON gate

50 nm

Super Steep Channel profile

Offset spacer

Gate 20nm

SiON Gete dielectric


Sub-micron CMOS with high-k gate

Cross-sectional TEM

CoSi$_2$

$V_d=1.0\ V$

$pMOS$

$nMOS$

$L_g=96\ nm$

$L_g=92\ nm$

$I_{on}=0.47\ mA/\mu m$ (NMOS)

$I_{on}=0.27\ mA/\mu m$ (PMOS)

Drain current ($A/\mu m$)

Gate voltage (V)
Review of MOS Capacitor: Band bending
nMOS (n-channel MOS): p-type Si sub.

- At accumulation,

Majority carriers are accumulated at the interface.
nMOS (n-channel MOS) : p-type Si sub.

◆ At depletion,

- No mobile carrier at the interface.

![Diagram showing charge density vs. gate voltage and energy levels]

- Gate voltage $V_g$ [V]
- Ions (Depletion charges)
- Energy [eV]

<table>
<thead>
<tr>
<th>Charge density [cm$^{-2}$]</th>
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<tr>
<td>$10^4$</td>
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- $V_g$ vs. Charge density |

- No mobile carrier at the interface.
nMOS (n-channel MOS) : p-type Si sub.

- At inversion, the gate voltage $V_g [V]$ increases, causing a huge change in the charge density. The reason for the high on/off ratio in MOSFETs is that minority carriers become majority at the interface.

Similar to n-doped at the surface, the charge density near the surface is more significant.

MOSFET characteristic is from this inversion layer.
nMOS (n-channel MOS): p-type Si sub.

- At inversion, surface charge obtained as a function of metal, oxide, and p-Si.

Energy [eV]:
- $E_c$, $E_v$, $E_i$, $E_i^\infty$, $E_F$.

Charge density [cm$^{-2}$]:
- Holes, Electrons, Ions.

Gate voltage $V_g$ [V]:
- $Q_{inv}$.

Surface charge obtained as a function of $V_g$. 

Diagram showing the transition from depletion to inversion and the corresponding charge density distribution.
nMOSFET
Operation Principle
Capacitance-Voltage Characteristics
n-MOSFET @ $V_{sd} = 0$ [V]

Holes cannot flow to source or drain (reverse biased).
n-MOSFET @ $V_{sd} = 0 \ [V]$

- **Source**: $n^+$
- **Drain**: $n^+$
- **p-type Si (Semiconductor)**
- **SiO$_2$ (Oxide)**

**Graphical Elements**
- **Energy [eV]**
- **Gate (Metal)**
- **Gate Voltage**: 0 V
- **SiO$_2$ (Oxide) Voltage**: 0 V
- **Depletion**
- **No mobile carriers. Ionized acceptors.**
- **No carrier (depleted) in the channel.**
n-MOSFET @ $V_{sd} = 0 \ [V]$

Oxide thickness is extremely thin ≈ 1.0 nm.

Inversion layer channel is formed.

Channel electrons are provided from source or drain.
Typical Capacitance-Voltage (C-V)

- **Electrons (Inversion)**: Inversion C-V is difficult to measure without source and drain electrodes.
- **Holes (Accumulation)**
- **Ions (depletion)**

**Al gate / SiO₂ / p-sub**

- $N_a = 1.0 \times 10^{17} \text{ [cm}^{-3}\text{]}$
- $t_{ox} = 1.0 \text{ [nm]}$
- $V_{FB} = -0.94 \text{ [V]}$
- $V_{th} = -0.037 \text{ [V]}$

This characteristics is observed in a MOSFET.
Linear & Sub-threshold regions
n-MOSFET @ $V_{sd} = 0.1 \, [V]$

- Gate (Metal)
- SiO$_2$ (Oxide)
- Accumulation (Holes)
- 0.1 V

Only limited leakage current can flow. (pn junction is reverse biased.)

Holes cannot flow to source or drain (reverse biased).
n-MOSFET @ $V_{sd} = 0.1$ [V]

Sub-threshold region (Very limited currents).

No carrier (depleted) in the channel.
n-MOSFET @ $V_{sd} = 0.1 \text{ [V]}$

Current flows between source and drain.

Energy [eV]

Gate (Metal)

SiO$_2$ (Oxide)

n-channel (electron) inversion layer

0.1 V

Gate

Source

Drain

0 V

$E_c$

$E_c$

Channel

Source $n^+$

Drain $n^+$

p-type Si (Semiconductor)

Linear region ($I_{ds} - V_{ds}$ characteristics are linear.)
Characteristics of 40-nm MOSFETs

\[ I_{on} = 0.68 \text{ mA/\mu m (NMOS)} \]
\[ I_{on} = 0.30 \text{ mA/\mu m (PMOS)} \]

@ \( I_{off} = 10 \text{ nA/\mu m, } V_d = 1.0 \text{ V} \)

PMOS

\[ V_g = 1.0 \text{ V} \]

NMOS

\[ V_g = -1.0 \text{ V} \]

Drain current \( I_d \) vs. \( V_d \) for \( V_g = 1.0 \text{ V} \) and \( V_g = -1.0 \text{ V} \).

Linear region

Sub-threshold region

\[ V_d = 0.05 \text{ V} \]

\[ V_d = 0.05 \text{ V} \]
Saturation Region: Pinch-off
n-MOSFET @ $V_{sd} = 2 \text{ [V]}$

On currents are saturated.
n-MOSFET @ $V_{sd} = 2$ [V]

Saturation region ($I_{ds}-V_{ds}$ characteristics are saturated.)

On currents are saturated.
Characteristics of 40-nm MOSFETs

\( I_{on} = 0.68 \text{ mA/}\mu\text{m} \) (NMOS)
\( I_{on} = 0.30 \text{ mA/}\mu\text{m} \) (PMOS)

@\( I_{off} = 10 \text{ nA/}\mu\text{m}, V_d = 1.0 \text{ V} \)

Saturated region

PMOS

NMOS

\( V_g = 1.0 \text{ V} \)

\( V_g = -1.0 \text{ V} \)

\( V_d = 0.8 \text{ V} \)

\( V_d = 0.6 \text{ V} \)

\( V_d = 0.4 \text{ V} \)

Saturated region
n-MOSFET @ $V_{sd} = 0 \ [V]$

- **Gate (Metal)**
- **SiO$_2$ (Oxide)**
- **Source $n^+$**
- **Drain $n^+$**
- **p-type Si (Semiconductor)**

nMOS uses electrons for a channel.
n-MOSFET

Off
$V_g = 0 \ [V]$ 

Sub-threshold
$0 < V_g < V_{th}$

Linear
$V_{th} < V_g$

Saturation
$V_{th} < V_g$

Current level changes significantly.
p-channel MOS Field-Effect-Transistor

Gate (Metal)

SiO$_2$ (Oxide)

Source $p^+$
n-type Si (Semiconductor)

Drain $p^+$

p-channel (hole) inversion layer

pMOS uses holes for a channel.
Linear & Sub-threshold regions of PMOSFET
p-MOSFET @ $V_{sd} = -0.1 \, [\text{V}]$

Energy and potential axes are opposite.

Only limited leakage current can flow.
(pn junction is reverse biased.)

Energy and potential axes are opposite.
p-MOSFET @ $V_{sd} = -0.1\ [V]$

Depletion
No mobile carriers. Ionized acceptors.

Sub-threshold region (Very limited currents).
No carrier (depleted) in the channel.
p-MOSFET @ $V_{sd} = -0.1 \ [\text{[V]}$]

Holes move from Source to Drain.

Linear region ($I_{ds}-V_{ds}$ characteristics are linear.)
Characteristics of 40-nm MOSFETs

$I_{on} = 0.68 \text{ mA/µm (NMOS)}$
$I_{on} = 0.30 \text{ mA/µm (PMOS)}$

@ $I_{off} = 10 \text{ nA/µm}, V_d = 1.0 \text{ V}$

Saturated region
p-MOSFET

Sign of the voltage will be opposite to n-MOS.

Source

Gate

Drain

Off
$V_{g} = 0 \ [V]$

Sub-threshold
$0 < -V_{g} < V_{th}$

Linear
$V_{th} < -V_{g}$

Saturation
$V_{th} < -V_{g}$
CMOS circuits

◆ NMOS

◆ PMOS

Both NMOS and PMOS are integrated.