ELEC3207 Nanoelectronic Devices

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Preparation: is there any difference?

- Apply 1V and 0V.
- Apply 10,001V and 10,000V.

Only the voltage difference matters!
Preparation: how about $pn$ diode?

◆ Apply 1V and 0V.

◆ Apply 0V and -1V.

Only the voltage difference matters!
Preparation: how about *this*?

- **Apply** -1V and 0V.
  - p⁺
  - n⁺
  - -1V
  - 0V
  - OFF

- **Apply** 0V and 1V.
  - p⁺
  - n⁺
  - 0V
  - 1V
  - OFF

Only the voltage difference matters!
Preparation: how about *this*?

- Apply 2V and 1V.
  - p⁺
  - 2V
  - n⁺
  - 1V

- Apply -1V and -2V.
  - p⁺
  - -1V
  - n⁺
  - -2V

Only the voltage difference matters!
Target device structure

Simplified version (sub-micron technology)
nMOSFET vs pMOSFET

◆ nMOSFET
  n-channel (electron)

◆ pMOSFET
  p-channel (hole)

Carrier polarity is opposite (electron ↔ hole).
Typical operation condition (ON)

◆ nMOSFET
n-channel (electron)

◆ pMOSFET
p-channel (hole)

Voltage is opposite (positive → negative).
Typical operation condition (ON)

◆ nMOSFET
  n-channel (electron)

◆ pMOSFET
  p-channel (hole)

Only the voltage difference matters (positive voltage)!!!
If we supply voltage to n-well,

- nMOSFET (ON)  
  n-channel (electron)

- pMOSFET (ON)  
  p-channel (hole)

Current does not flow under the reverse bias.

we can use the same p-type substrate.
nMOSFET vs pMOSFET

◆ nMOSFET
n-channel (electron)

◆ pMOSFET
p-channel (hole)

This is the target FETs.
How to apply the voltage to the well?

- pMOSFET with well (body, back) contact

We will need additional 2 masks for doping.
Mask layout for pMOSFET

- pMOSFET with well (body, back) contact

7 masks required (L, NW, FG, N, P, CONT, M1).
Front-end process (non-metal) 
pMOS FET 
Fabrication Flow

I will just highlight the difference between pMOS and nMOS.
pMOSFET

- Plan view
- Cross section

Final structure.
Device Isolation

Electrically isolate devices for integrations
Surface Cleaning

◆ Plan view

◆ Cross section

$\rho$-Si

$\rho$-Si

Surface preparation
Oxidation

◆ Plan view

◆ Cross section

SiO$_2$/p-Si

Surface protection
Oxidation

◆ Plan view

◆ Cross section

Si$_3$N$_4$/SiO$_2$/p-Si

Surface protection
The first lithography (L) & dry etching
◆ Plan view

◆ Cross section

Si₃N₄/SiO₂/p-Si

Si₃N₄/SiO₂ Active field (device area) p-Si

Active field definition
CVD SiO$_2$ deposition or Spin-On-Glass coating

◆ Plan view

SiO$_2$/Si$_3$N$_4$/SiO$_2$/p-Si

◆ Cross section

Electrical isolation by filling the oxide (insulator).
Chemical-Mechanical-Polishing (CMP)

◆ Plan view

◆ Cross section

Si₃N₄/SiO₂/p-Si

Si₃N₄
SiO₂
Active field (device area)
p-Si

Planarization.
Cleaning the surface

◆ Plan view

STI

◆ Cross section

STI

p-Si

p-Si

Shallow Trench Isolation (STI) completed.
n-Well formation

In order to integrate both nMOS and pMOS on the same substrate towards CMOS (complementary MOS)
To protect the surface.
Resist patterning and ion implantation (NW)

Plan view

Cross section

P (phosphorous) or As (arsenide) will be implanted.
P or As will be activated to form n-well.
Gate formation

The most important process for CMOS
Thermal oxidation or high-k deposition

- Plan view

- Cross section

The most important process for MOSFET.
Poly-Si deposition

Plan view

Poly-Si/SiO$_2$/n$^-$ Si/p$^-$ Si

Cross section

STI

n$^-$ Si

Poly-Si

STI

p$^-$ Si

CVD
Lithography & dry etching for gate patterning (FG)

Plan view

Cross section

The most important patterning (minimum feature).
Self-aligned
Source-Drain formation

We will use self-aligned process, but still we need a resist mask (P).

Make the source-drain just below the gate as close as possible.
Resist mask patterning (P)

◆ Plan view

◆ Cross section

We will make pMOSFET.
Resist mask patterning (P)

- Plan view

- Cross section

B (boron) will be implanted.
Self-aligned Source-Drain & Gate

- **Plan view**

- **Cross section**

Resist removal & cleaning.
Resist mask patterning for n-well contact (N)

- Plan view

- Cross section

P (phosphorous) or As (arsenide) will be implanted.
Annealing (@~1000°C) for impurity activation

◆ Plan view

◆ Cross section

Front end process completed.
Back-end process (metal)

Self-Aligned siLICIDE (SALICIDE)

No mask needed

Make the metallic contact very close to the source, drain, and gate electrodes.
CVD SiO2 deposition & Reactive-Ion-Etching (RIE)

◆ Plan view

◆ Cross section

Side-wall spacer formed to avoid short circuits.
Deposit metal (Co, Ti, or Ni) & anneal(@~500°C)

◆ Plan view

◆ Cross section

Self-Aligned siLICIDE (SALICIDE)
Metal contact for circuits

2 masks (CONT, M1) needed.
SiO2 deposition + CMP + Lithography + Dry (CONT)

- Plan view

- Cross section

Contact opening.
The first metal layer deposition & patterning (M1)

◆ Plan view

◆ Cross section

Continue several metallic layers (up to 5 - 10 layers)
PMOS FET
Mask Layout
Summary for the layout & key process

- Mask Layout

1. STI or LOCOS (L)
2. N-Well (NW)
3. First Gate (FG)
4. Source & Drain (P)
   - Ion implantation
5. Body contact (N)
   - Ion implantation
6. SALICIDE
7. Metal contact (CONT)
8. Metal patterning (M1)

Extra mask for pMOS: NW
Summary for the layout & key process

**Mask Layout**

1. STI or LOCOS (L)
2. N-Well (NW)
3. First Gate (FG)
4. Source & Drain (P)
   
   Ion implantation
5. Body contact (N)
   
   Ion implantation
6. SALICIDE
7. Metal contact (CONT)
8. Metal patterning (M1)

Extra mask for pMOS: NW, P, N
Summary for the layout & key process

1. Field preparation (L)
   Shallow trench Isolation (STI) or Local-oxidation-of-Si (LOCOS)

2. First Gate (FG)
   Gate (SiO2 or high-k) dielectric Poly-Si or metal gate

3. Source& Drain (no mask)
   Self-aligned ion implantation Sidewall patterning Silicidation

4. Metal contact (CONT)
   Chemical-Mechanical-Polishing (CMP)

5. Metal patterning (M1)

About 100 processes required.