Advanced Computer Architecture
ELEC3219 (2017/18)

Busses

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What is a Bus?

• A communication pathway connecting two or more devices
• Usually broadcast (all components see signal)
• Often grouped
  – A number of channels in one bus
  – e.g. 32 bit data bus is 32 separate single bit channels
• Power lines may not be shown
Data Bus

• Carries data
  – Remember that there is no difference between “data” and “instruction” at this level
• Width is a key determinant of performance
  – 8, 16, 32, 64 bit

Where is this bus?
Address bus

• Identify the source or destination of data
  – CPU needs to read an instruction (data) from a given location in memory

• Bus width determines maximum memory capacity of system
  – e.g. 8080 has 16 bit address bus giving 64k address space

Where is this bus?
Control Bus

• Control and timing information
  – Memory read/write signal
  – Interrupt request
  – Clock signals

Where is this bus?
Bus Interconnection Scheme

- CPU
- Memory
- Input and Output

- Control bus
- Address bus
- Data bus

System bus
Single Bus Problems

• Lots of devices on one bus leads to:
  – Propagation delays
    • Long data paths mean that co-ordination of bus use can adversely affect performance
    • If aggregate data transfer approaches bus capacity

• Most systems use multiple buses to overcome these problems
Traditional Industrial Standard Architecture (with cache)
High Performance Bus
Bus Types

• Dedicated
  – Separate data & address lines

• Multiplexed
  – Shared lines
  – Address valid or data valid control line
  – Advantage - fewer lines
  – Disadvantages
    • More complex control
    • Ultimate performance
Bus Arbitration

- More than one module controlling the bus
  - e.g. CPU and DMA controller
- Only one module may control bus at one time
- Arbitration may be centralised or distributed
Centralised Arbitration

- Single hardware device controlling bus access
  - Bus Controller
  - Arbiter
- May be part of CPU or separate
Distributed Arbitration

- Each module may claim the bus
- Control logic on all modules
Timing

• Co-ordination of events on bus
• Synchronous
  – Events determined by clock signals
  – Control Bus includes clock line
  – A single 1-0 is a bus cycle
  – All devices can read clock line
  – Usually sync on leading edge
  – Usually a single cycle for an event
Synchronous Timing Diagram
Asynchronous Timing – Read Diagram

- Status lines
  - Status signals

- Address lines
  - Stable address

- Read

- Data lines
  - Valid data

- Acknowledge
Asynchronous Timing – Write Diagram
Questions
PCI Bus (Optional)

• Peripheral Component Interconnection (PCI)
• Intel released to public domain
• 32 or 64 bit
• 50 lines
PCI Bus Lines (required)

- **Systems lines**
  - Including clock and reset
- **Address & Data**
  - 32 time mux lines for address/data
  - Interrupt & validate lines
- **Interface Control**
- **Arbitration**
  - Not shared
  - Direct connection to PCI bus arbiter
- **Error lines**
PCI Bus Lines (Optional)

• Interrupt lines
  – Not shared
• Cache support
• 64-bit Bus Extension
  – Additional 32 lines
  – Time multiplexed
  – 2 lines to enable devices to agree to use 64-bit transfer
• JTAG/Boundary Scan
  – For testing procedures
PCI Commands

• Transaction between initiator (master) and target
• Master claims bus
• Determine type of transaction
  – e.g. I/O read/write
• Address phase
• One or more data phases
PCI Read Timing Diagram

CLK

FRAME#

AD

ADDRESS

DATA-1

DATA-2

DATA-3

C/BE#

BUS CMD

Byte Enable

Byte Enable

Byte Enable

IRDY#

Wait

Wait

Wait

Wait

Wait

TRDY#

Data Transfer

Data Transfer

Data Transfer

Data Transfer

DEVSEL#

Address Phase

Data Phase

Data Phase

Data Phase

Bus Transaction
PCI Bus Arbitration

CLK
REQ#-A
REQ#-B
GNT#-A
GNT#-B
FRAME#
IRDY#
TRDY#

Address Data

access-A

Address Data

access-B
Question?