Advanced Computer Architecture
ELEC3219 (2017/18)

Wires and Busses
(Examples)

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• What are the AHB, ASB and APB
• How many bits for the Busses?
• Does it have a synchronous interface?
• Address, date and control, are they combined or separated using different bits?
• Does it have Master and slave?
OpenCores Wishbone Bus

• Does it have Master and Slave
• What kind of design is it?
• How many bits for the Busses?
• Does it have a synchronous interface?
• Address, date and control, how do they design?
IBM CoreConnect (supported by Xilinx)

- Does it have Master and Slave?
- What kind of design is it?
- How many bits for the Busses?
- Does it have a synchronous interface?
- Address, date and control, how do they design?
Altera Avalon

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Open Core Protocol

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• Question?