Advanced Computer Architecture
ELEC3219 (2017/18)

Wires and Busses
(Examples)

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AMBA

• What does AMBA look like?
• What are the AHB, ASB and APB
• How many bits for the Busses?
• Does it have a synchronous interface?
• Address, date and control, are they combined or separated using different bits?
• Does it have Master and slave?
OpenCores Wishbone Bus

• What does OpenCores Wishbone Bus look like?
• Does it have Master and Slave
• What kind of design it is?
• How many bits for the Busses?
• Does it have a synchronous interface?
• Address, date and control, how do they design?
IBM CoreConnect (supported by Xilinx)

- What does the IBM CoreConnect look like?
- Does it have Master and Slave
- What kind of design it is?
- How many bits for the Busses?
- Does it have a synchronous interface?
- Address, date and control, how do they design?
Altera Avalon

• What does Altera Avalon look like?
• Does it have Master and Slave
• What kind of design it is?
• How many bits for the Busses?
• Does it have a synchronous interface?
• Address, date and control, how do they design?
OpenCore Protocol

• What does OpenCore Protocol look like?
• Does it have Master and Slave
• What kind of design it is?
• How many bits for the Busses?
• Does it have a synchronous interface?
• Address, date and control, how do they design?