Introduction

The Intersil ISL37300P WLAN PC card is a complete wireless high speed Network Interface Card (NIC) utilizing the Intersil PRISM® 2.5 Direct Sequence Spread Spectrum (DSSS) Wireless Transceiver chip set. It provides a complete PRISM 2.5 reference design evaluation platform of hardware and software to system providers or integrators requiring wireless data communications capability and is ideal for integration into computer platforms.

A complete PRISM chipset WLAN reference design package (ISL37300P-CD) or an evaluation kit (ISL37300P-EVAL) are available. The reference design package contains all the documentation needed for manufacturing of the PRISM 2.5 PCMCIA wireless network card including: Cadence/Allegro Layout, Gerber files, concept schematic, Bill of Materials, assembly and mechanical drawings, test plan, and even a copy of the application for FCC equipment authorization. Customers who license the reference design also receive password access to Intersil's Premier website for up to the minute updates on hardware and software.

The evaluation kit (ISL37300P-EVAL) includes two WLAN PC cards designed to Intersil's PRISM reference design, Microsoft® Windows® driver, local area network evaluation software, PRISM test utilities (PTU) software and documentation to complete the evaluation. It supports the IEEE802.11b network specification for DSSS signaling, providing data rates of 1, 2, 5.5, and 11Mbps. Evaluation kit software updates are available on the Intersil website.

Figure 1 shows a block diagram of the reference radio design. This radio has been designed to conform to the IEEE802.11b standard.

This application note details the RF and analog design of these cards giving a detailed description of the receive and transmit processes.

General Specifications

- Targeted Standard ..................... IEEE802.11b
- Data Rate ........................... 1Mbps DBPSK
  2Mbps DQPSK
  5.5Mbps CCK
  11Mbps CCK
- Range .............................. 300 ft Indoor (Typ)
  1750 ft Outdoor (Typ)
  - Frequency Range ................. 2412–2484MHz
  - Step Size ........................ 1MHz
  - IF Frequency ........................ .374.25MHz
  - IF Bandwidth .................... 17MHz
  - Operating Voltage ............... 3.3V
  - IEEE802.11 Power Save Mode .... 62mA
  - Operating Temperature Range .... 0°C to 70°C
  - Storage Temperature Range ...... -20°C to 85°C
  - Mechanical ........................ Type II PC Card
  - Antenna Interface ................... PCB antennas on card
  - Moisture Rating (See [7]) ......... ISL3873 LVL3, 168 hr
  HFA3783 LVL3, 168 hr
  ISL3685 LVL3, 168 hr
  ISL3984 LVL2, 1 yr
  ISL3183 LVL1, unlimited

Receive Specifications

- Sensitivity ......................... -93dBm (Typ), 1Mbps, 8E-2 FER (Note 1)
  -90dBm (Typ), 2Mbps, 8E-2 FER (Note 1)
  -89dBm (Typ), 5.5Mbps, 8E-2 FER (Note 1)
  -85dBm (Typ), 11Mbps, 8E-2 FER (Note 1)
  - Input Third Order Intercept Point (high gain) .. -9.5dBm (Typ)
  - Image Rejection .................... 45dB (Typ)
  - IF Rejection ........................ >84dB (Typ)
- Adjacent Channel Rejection .......... 53dB (Typ)
- Rx Supply Current .................... 205mA (Typ)

Transmit Specifications

- Output Power ........................ +16dBm (Typ)
- Transmit Spectral Mask (IEEE802.11b) .......... 30dBc at first sidelobes
- Tx Supply Current .................... 290mA (Typ)

NOTE:
1. FER = Frame Error Rate or Packet Error Rate.
FIGURE 1. WIRELESS LAN PC CARD BLOCK DIAGRAM

NOTE: Both 2 and 4Mbit Flash supported
FIGURE 2. WIRELESS LAN PC CARD TEST POINTS
**Receive Processing**

The signal is received through either one of the two antennas on the card as shown in the block diagram of Figure 1. These two antennas are controlled by the ISL3873 MAC/BBP chip and the T/R switch. Antenna diversity is used to counter the adverse effects of multipath fading and antenna pattern nulls. Such advantages justify the extra space that the second antenna occupies on the card. The received input from the antenna passes through a bandpass filter (FL6), which is used to provide protection for the RF front-end from out of band interfering signals, and it also provides image rejection for the first downconverter.

The signal then enters the receive chain of the ISL3685 RF/IF Converter which features a low noise, selectable-gain amplifier (LNA). This amplifier is used to set the receiver noise figure (NF). The LNA section of the ISL3685 has a selectable gain control H/L pin (pin #5). When the MAC/Baseband processor detects the presence of a strong signal from the IF peak detector output of the HFA3783, it will change the gain settings of the LNA in ISL3685. The peak detector threshold limit is typically -20dBm at the input of the radio. This gain control feature further improves the dynamic range and the intermodulation performance of the PRISM 2.5 Chip set. The LNA and its output matching are designed to provide required image noise rejection.

After the LNA the signal enters the mixer section of the ISL3685, where down-conversion from the RF frequency of 2.4–2.5GHz band is performed. The IF frequency is 374.25MHz. Low-side injection is used to place the received image 748.5MHz below the tuned channel. The down converter is driven by an external RF LO with its frequency of operation phase locked by a PLL internal to the ISL3685. This PLL circuit uses an external 44MHz crystal oscillator as a reference frequency input. It should be noted that the ISL3685 RF/IF converter operates from two separate regulated 2.84V supplies. One regulator, VCCA, supplies the receive and transmit section of the chip, while the other, VCCB, is dedicated to the PLL section and the external RF LO.

The output of the RF/IF converter is a differential pair of IF signals (RX_MX_OUT+, RX_MX_OUT-). These two signals are open collector with high impedance outputs. They are designed to share a common IF matching network and an IF SAW filter with the transmit mixer. The PC board layout was designed with care to avoid interference and noise pickup. Layout symmetry and management of PC board parasitics was also taken into consideration in order to maximize the bandwidth of the IF matching network.

A standard LC matching network consisting of R39, R44, L12, L14, C49, and C75 was used at the output of the ISL3685 in order to match the output to 200Ω differential. The differential signals are then fed into an IF SAW filter, FL1, with center frequency of 374MHz, and a 3dB bandwidth of 20MHz. The group delay variation of this filter is typically 40ns and the insertion loss is typically 8.5dB. The filter’s differential inputs are matched to 200Ω using L5, C39 and C44. Another LC matching network was designed using L6, C45 and C46 in order to match the output of the SAW filter to 200Ω. This is required to interface with the IF demodulator chip.

The SAW filter is used to suppress adjacent channel interference generated by other in-band sources. The insertion loss is not critical, since at this point in the receiver, component loss or NF is offset by the preceding gain stages. It is worth emphasizing the fact that careful design of the ISL3685 RF/IF Converter TX/RX interface as well as design of the HFA3783 IQ Modulator/Demodulator TX/RX interface provided a possibility to share a single SAW filter in a receive and transmit mode. This approach reduces the cost of the Bill of Materials (BOM) with the PRISM 2.5 radio chip set.

The differential filter outputs are then fed to the I/Q modulator/demodulator chip (the HFA3783). In the receive

<table>
<thead>
<tr>
<th>STAGE</th>
<th>G</th>
<th>F</th>
<th>IP3O</th>
<th>GC</th>
<th>FC</th>
<th>IP3OC</th>
<th>IP3IC</th>
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<td>-0.5</td>
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<td>43.0</td>
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<td>39.7</td>
<td>40.7</td>
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<td>FL6 Receive Band Filter</td>
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<td>2.0</td>
<td>100.0</td>
<td>-3.0</td>
<td>3.0</td>
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<td>LNA</td>
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<td>8.0</td>
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<td>20.7</td>
<td>6.1</td>
<td>13</td>
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<td>100.0</td>
<td>12.2</td>
<td>6.2</td>
<td>4.6</td>
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<td>8.0</td>
<td>42.2a</td>
<td>68.2</td>
<td>6.5</td>
<td>42.1</td>
<td>-26.1</td>
</tr>
</tbody>
</table>

Cascaded Gain = 68.2dB  Cascaded NF = 6.5dB  Cascaded Output IP3 = 42.1dBm

Assumed input power level: -100dBm

**NOTE:** G (individual stage gain, dB), F (NF, dB), IP3O (individual stage output IP3, dBm), GC (cumulative gain, dB), FC (cumulative NF, dB), IP3OC (cumulative output IP3, dBm), IP3IC (cumulative input IP3, dBm).

a. Calculated here is out-of-band IP3 performance (two jammers outside the IF filter passband and one 3rd order IM product inside). The underlying assumption is that the IP3O of the IF strip is improved by the rejection of the jammers by the preceding filter.
mode, the differential signals travel through two cascaded, low distortion, integrated AGC IF amplifiers. Following the AGC stages, an AC coupled down-conversion pair of quadrature doubly balanced mixers are used for I and Q demodulation. The output of the I and Q mixers are DC coupled to a pair of anti-aliasing baseband filters with DC offset correction. The down converter mentioned above is driven by a broadband quadrature IF LO generator with frequency of operation phase locked by a PLL provided by Intersil's integrated external IF VCO (ISL3183) and HFA3783. This PLL circuit contains a three-wire interface for serial bus programming. The 44MHz crystal oscillator mentioned above is also used as the reference frequency source for this PLL. The HFA3783 operates from two separate regulated 2.84V supplies. One regulator, VCCA, supplies the receive and transmit section of the chip, while the other, VCCB, is dedicated for the PLL section and the external IF LO. The cascaded front end noise figure, IP3 and gain distribution analysis are shown in Table 1.

The balanced differential analog outputs of the HFA3783 signals (RxI+, RxI-, RxQ+, RxQ-) are then fed into the BBP section of the combined MAC/BBP chip (ISL3873). The shape of the received I and Q analog baseband signals are shown in Figure 3. In the receive path, these signals enter the two on-board 6-bit analog to digital converters (A/Ds). An AGC circuit is designed to adjust for signal level variations and to optimize A/D performance of the I and Q inputs by providing proper headroom on the 6-bit converters. The 44MHz crystal oscillator, previously mentioned, is used to provide the main clock for the ISL3873.

The balanced differential analog outputs of the ISL3873 signals are used to provide the spreading function. The baseband processor correlates the PN sequence, adjusting its carrier and symbol timing to lock onto the signal and uncover the packet data. The receiver section operates on the RAKE receiver principle, which maximizes the signal to noise ratio (SNR) of the signal by combining the energy of multipath signal components. The RAKE receiver is implemented with a channel matched filter (CMF) using a finite-duration impulse response (FIR) filter structure with 16 taps. The CMF is programmed by calculating the channel impulse response (CIR) and mathematically manipulating the tap coefficients. Thus, the CMF compensates for channel distortion characteristics such as multipath and optimizes the signal for minimum inter-symbol interference (ISI). Since the calculation of the impulse response is inaccurate at low signal to noise or in the presence of a strong continuous wave (CW) interference, the chip has thresholds (CR36 to CR39) that are set to substitute a default CMF shape under these conditions.

The RAKE receiver contains 16 correlation ‘fingers’ that are evenly spaced at 1/2 chip intervals. The RAKE receiver aligns correlation peaks on the fingers and sums them to optimize the SNR in the presence of multipath. The ISL3873 also employs a decision feedback equalizer (DFE) at the output of the RAKE receiver that updates the CMF for the next receive bit. The combination of these two functions acting in concert, optimize the SNR of the received signal in the presence of multipath fading while minimizing the ISI of signal at the same time.

Following the channel filters, there are two types of correlators in the ISL3873 baseband processor. The first is a parallel matched filter correlator that searches for the Barker sequence used in the preamble, header, and PSK data modes. These modes are DBPSK modulation used for 1Mbps data rate while DQPSK is used for 2Mbps. The correlator despreads the samples from the chip rate back to the original symbol rate giving 10.4dB processing gain for 11 chips per symbol. While despreading the desired signal, the correlator spreads out the energy of any non-correlating interfering signal thus providing greater resistance to jamming.

The second form of correlator is the parallel correlator bank used for detection of the complementary code keying (CCK) modulation for either 5.5Mbps or 11Mbps data rates. Data is encoded into orthogonal PN sequences used instead of a fixed Barker code. Each correlator of the bank searches for a specific pseudo random sequence resulting in two decoded bits for 5.5Mbps and six decoded bits for 11Mbps. The detected output is then processed through the differential phase decoder to demodulate the last two bits of each symbol.
The packet header contains a start frame delimiter (SFD), other signal related data and a cyclic redundancy check (CRC) for data error detection. The MAC processes the header data to locate the SFD, determine the mode and length of the incoming message and to check the CRC. The MAC then processes the packet data and sends it on through the PCI interface to the host computer. The PCI host interface allows access to the ISL3873 memory and host registers using memory read or write transactions. If corrupt data is detected, the MAC requests a re-transmission of the packet.

The IEEE802.11b WLAN MAC protocol is implemented with the on board firmware. The MAC firmware supports ad hoc and infrastructure operation as well as low level protocols such as request to send (RTS), clear to send (CTS) generation and acknowledgement. Additional features include: fragmentation, de-fragmentation, and automatic beacon monitoring are handled without host intervention. Active scanning is performed autonomously once initiated by host command, while host interface commands and status handshakes allow concurrent operation from multi-threaded I/O drivers. Additional firmware functions specific to access point applications are also available. The ISL3873 MAC/BBP chip operates from the PC card bus 3.3V supply.

Transmit Processing

Data from the host computer is sent to the MAC section of the ISL3873 chip via the PC card interface. Prior to any communication, the MAC sends an RTS packet to the other end of the link and in turn, receives a CTS packet. The MAC then formats the payload data packet (MPDU) by appending to it a preamble and header. This is then sent to the BBP section of the same chip which clocks it in.

The packet will then be processed along two different paths depending on the modulation used. For 1- and 2Mbps modes, the transmitter accepts data from the external source, scrambles it, differentially encodes it as either DBPSK or DQPSK [11] respectively, and spreads it with the PN sequence. The BPSK and QPSK spreading is performed using an 11-chip Barker sequence and is modulated with I and Q data components.

While employing the complementary code keying (CCCK [14]) modes, the output of the scrambler is partitioned into nibbles (4 bits) or bytes (8 bits). At 5.5Mbps, it uses two of those bits to select one of four complex spread sequences from a table of CCK sequences and then QPSK modulates that symbol with the remaining two bits. Thus, there are four possible spread sequences to send at four possible carrier phases, but only one is sent. The sequence is then modulated on the I and Q output. At 11Mbps, one byte is used in a similar method as at 5.5Mbps, where 6 bits are used to select one of 64 spread sequences for a symbol, and the other two are used to QPSK modulate that symbol. Therefore, there are in total 256 possible combinations of sequence and carrier phases, with only one being sent. Again, the sequence is modulated on the I and Q output. All the above data rates are implemented with an 11MHz chip rate using a 44MHz clock.

The scrambler is used for the preamble, header and data in all modes. The preamble is always transmitted as the DBPSK waveform, while the header can be configured to either be DBPSK, or DQPSK. Data packets can be configured for either DBPSK, DQPSK, or CCK. The preamble is used by the receiver to achieve initial pseudo noise (PN) synchronisation, while the header includes the necessary data fields for the communications protocol to establish the physical layer link. The transmitter generates the synchronization preamble and header and knows when to make the DBPSK to DQPSK or CCK switchover, as required.

The modulator output is the balanced differential analog signals (TXI+, TXI-, TXQ+, TXQ-).

Transmit AGC uses a 7-bit DAC control to obtain maximum performance in the analog portions of the transceiver. As mentioned previously in the Receiver Processing section, the ISL3873 MAC/BBP chip operates from a 3.3V supply.

The HFA3783 modulator section has an I/Q baseband bandwidth of DC to 13MHz (typ) and IF frequency range of 70–600MHz. It consists of differential I and Q baseband inputs requiring pre-shaped analog data levels up to
500mVpp. A common mode voltage of around 1.3V is required for proper operation of the four differential input pins. There are no internal pre-shaping filters in the modulator section. Following the differential input stages, a DC coupled up-conversion pair of quadrature doubly balanced mixers are used for I and Q baseband IF processing. These differential mixers are driven by the same internal IF LO quadrature generator used in the receive section. Their phase and gain characteristics, including I/Q matching, are well suited for accurate data transmission. The final stage is an AGC differential amplifier with 70dB of dynamic range. The output is a differential, open collector signal (IF_TX+, IF_TX-) which requires DC bias from VCC through an inductor. A matching network was designed at the differential output path of the HFA3783 in order to balance it to 200\(\Omega\). This network consists of R40, L9, L10, C51 and C52. The differential signals are fed into a bandpass IF SAW filter, FL1. This is the same filter used in the receive path of the PRISM 2.5 radio. The IF SAW filter shapes the transmit spectrum and rejects any spurs generated in the transmit section of the HFA3783. The effect of the IF SAW filter on transmit signal spectrum is displayed in the Figures 5 and 6.

The output of the SAW filter then enters the RF/IF Converter (ISL3685). This differential pair of IF signals (Tx_mx_in+, Tx_mx_in-) are self biased, high impedance inputs requiring AC coupling. The differential input path into the ISL3685 is also balanced to 200\(\Omega\) by using C47 and C74.

The transmit path of the signal side the ISL3685 consists of an up-converter mixer and a high performance preamplifier (approx. 15.6dB of gain at 2.45GHz). This preamplifier aids in easing the requirement for ISL3984 RFPA gain. The up-converter is driven by the same RF VCO and PLL used in the receive path of PRISM 2.5. No external filtering is required between the RF upconverter and the TX preamplifier due to the LO and image rejection designed into the IC.

The output of the RF/IF converter is a single ended signal (TXA_OUT). The signal is then fed into two MURATA bandpass filters, FL4 and FL5. These filters help suppress the LO feedthrough from the mixer and any undesired mixing products.

This RF signal is then sent to the ISL3984 single supply SiGe RF power amplifier. At this point in the transmit chain, the output spectrum contains no sidelobes as the SAW IF filter has removed them (see Figure 6). The image-reject up-converter and amplifiers operate in their linear region and produce no spectral regrowth. This allows the ISL3984 to be the sole contributor to spectral regrowth, which allows the PA to operate as close as possible to the 1dB compression point with minimum back-off. This maximizes the power efficiency of the overall design. A typical output frequency spectrum showing -30dBc sidebands is shown in Figure 7. The ISL3984 delivers 18dBm (typ) of output power while meeting ACPR specification of less than -30dBc (1\textsuperscript{st} sidelobe) and less than –50dBc (2\textsuperscript{nd} sidelobe). In addition, the device includes a 2.4GHz power detector, which is accurate over a 15dB dynamic range within ±1dB which supports an accurate automatic level control (ALC) function. Following the RFPA, a low pass filter (FL3) is used to attenuate high frequency harmonics of the desired signal and LO. The insertion loss of FL3 is approximately 0.5dB. The T/R switch also exhibits a loss of 0.5dB so the amount of transmit power available at the test point E is approximately +17dBm.

As mentioned in the Receive Processing Section, the BBP section of the ISL3873 chip is in charge of controlling the antenna diversity. Diversity is only provided in receive mode. Transmitted signals must use the AN1 antenna. The BBP continuously checks the channel to receive any incoming
data from the reference transmitter. However, if the channel is clear and there is no data to receive, it enables AN1 to transmit any outgoing data. Therefore, by default, the WLAN card is always in receive mode. This is done to avoid collisions of incoming and outgoing data.

The final output spectrum can be seen in Figure 7. The center frequency of this signal is 2412–2484MHz depending on the channel of operation. The sidelobes of the spectrum are adjusted by the ALC/AGC to be 30dB below the main peak of the spectrum per requirements of IEEE802.11b.

**Synthesizer Section**

Two local oscillators are used in the PRISM 2.5 WLAN PC card design. The RF LO consists of the RF VCO U14 and the synthesizer which is internal to the RF/IF Converter (ISL3685). The RF output of the RF VCO is buffered using U16 (UPC2745TB buffer amplifier). This amplifier will help reduce pulling effects on the first LO, especially when the RF front end switches between the RX and TX mode of operation.

The loop filter for the RF PLL is made from C118, C123, R69, R65 and C125. Measurement of the phase noise and calculation of integrated RMS phase jitter are included in Appendix A. The RF LO input of the ISL3685 is internally AC coupled and matched to 50Ω. The behavior of the RF VCO can be monitored at test point F and is shown in Figure 8. Ideally, the tuning voltage of the VCO, when locked, falls between 0.5V and 2.2V. The tuning voltage of the RF VCO can be observed at test point G.

The IF LO consists of the IF VCO, U13 (ISL3183) and the synthesizer which is internal to the I/Q modulator/demodulator (HFA3783). The second synthesizer is programmed to the fixed frequency of 748.5MHz. The output of the IF VCO is fed differentially back into the HFA3783 (U9). This differential IF signal is divided by 2 in U9 to yield the IF LO frequency of 374.25MHz. This LO is applied to the I/Q modulator/demodulator section of the HFA3783. The loop filter for the IF PLL is made from C91, C100, R52, R55 and C107. Phase noise measurement and calculation of integrated RMS phase jitter are included in Appendix A. The behavior of the IF VCO can be monitored at test point H and is shown in Figure 9.

It should be noted that both synthesizers are using the same 44MHz reference frequency crystal oscillator, U6.
Handling and Processing Moisture Sensitive Surface Mount Devices

Certain plastic encapsulated surface mount devices (SMDs) if not handled properly can incur damage during the solder reflow attachment process to printed circuit boards (PCBs). The damage occurs as a result of internal package cracking (commonly referred to as popcorn cracking) and/or delamination between internal package interfaces.

The root cause of this type of failure mechanism is the rapid heating of the moisture absorbed within the plastic encapsulant. All plastic packages absorb moisture. During typical solder reflow operations when SMDs are mounted onto a PCB, the entire PCB and device population are exposed to a rapid change in ambient temperature. Any absorbed moisture is quickly turned into superheated steam. This sudden change in vapor pressure can cause the package to swell. If the pressure exerted exceeds the flexural strength of the plastic mold compound, then it is possible to crack the package. Even if the package does not crack, interfacial delamination can occur.

If a particular package style is determined to be moisture sensitive, then the product must be shipped in dry pack. The dry pack bag is a tough, moisture resistant bag. Placed inside a dry pack bag along with predetermined amount of desiccant and a humidity sensitive indicator card. Upon opening a dry pack bag with product, the user needs to check two items:

- the seal date on the label, and
- the moisture indicator from within the bag.

If the bag seal date is over one year and/or the humidity indicator card shows greater than 20% RH, the product needs to be re-baked prior to reflow.

If a rework of a PCB with moisture sensitive SMDs is required, special precautions must be observed. Should the rework require complete exposure of the PCB to reflow conditions, then the manufacturer needs to take into account the shortest floor life of any moisture sensitive SMD on the board. If the floor life has been surpassed, then the entire board should be re-baked.

Detailed information on classification and handling instructions can be found in TB363 Tech Brief, Guidelines for Handling and Processing Moisture Sensitive surface Mount Devices [7].

Frequency Assignment

<table>
<thead>
<tr>
<th>CHANNEL NUMBER</th>
<th>CHANNEL FREQUENCY</th>
<th>GEOGRAPHIC USAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2412MHz</td>
<td>US, CA, ETSI, MKK</td>
</tr>
<tr>
<td>2</td>
<td>2417MHz</td>
<td>US, CA, ETSI, MKK</td>
</tr>
<tr>
<td>3</td>
<td>2422MHz</td>
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<td>14</td>
<td>2484MHz</td>
<td>MKK</td>
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</table>

KEY:
US = United States, CA = Canada, ETSI = European countries (except France and Spain), FR = France, SP = Spain, MKK = Japan

Table 2 delineates the IEEE802.11 channels and their corresponding center frequencies. Although information contained in Table 2 is deemed to be accurate, local regulatory authorities should be consulted before using such equipment.

**FCC Information to user**

This product does not contain any user serviceable components and is to be used with approved antennas only. Any product changes or modifications will invalidate all applicable regulatory certifications and approvals.

**FCC Radiation Exposure Statement**

This device generates and radiates radio-frequency energy. In order to comply with FCC radio-frequency radiation exposure guidelines for an uncontrolled environment, this equipment should be installed and operated with the minimum distance between your body and the antenna as shown in the table below.

**FCC Electronic Emission Notices**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference

(2) This device must accept any interference received, including interference that may cause undesired operation.
FCC Radio Frequency Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Guidelines for Human Exposure

The EIRP was measured for the lower, middle and highest frequencies used by the transmitter. The results in Table 3 are based on a safe distance between antenna and operator of eight inches. The equipment therefore fulfills the requirements on power density for general population / uncontrolled exposure of 1.0 mW/cm^2 and therefore complies with the requirements of FCC Part 15.247 (b) (4) and FCC OET Bulletin 65 including supplements A, B and C.

<table>
<thead>
<tr>
<th>TABLE 3. POWER DENSITY CALCULATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured EIRP (mW)</td>
</tr>
<tr>
<td>---------------------</td>
</tr>
<tr>
<td>74.1</td>
</tr>
<tr>
<td>Calculated Power Density (mW/cm^2)</td>
</tr>
</tbody>
</table>

3.3V PC-card Interface Standard

**CAUTION:** This assembly is designed to operate with a supply voltage of 3.3V in laptop computers supporting the PC card standard. This card is equipped with a hardware key to prevent improper insertion into a 5V only slot.

**CAUTION:** Do not force engagement of the card in the PC card slot. It is mechanically designed to prevent improper insertion. Permanent damage may occur if operated outside of the specified operating limits listed in this document.

Bill Of Materials (BOM)

The most up to date BOM can be found on the Premier website.

http://www.intersil.com/prism/software

Reference Documents

[1] ISL3873 Data Sheet, Intersil Corporation
[2] ISL3685 Data Sheet, Intersil Corporation
[3] ISL3984 Data Sheet, Intersil Corporation
[4] HFA3783 Data Sheet, Intersil Corporation
[5] ISL3183 Data Sheet, Intersil Corporation
[13] TB395, Tech Brief, Intersil Corporation, RF Probing of the ISL37300P and the ISL37300XU
[16] AN9633, Application Note, Intersil Corporation, Processing Gain for Direct Sequence Communication Systems and PRISM
[17] TB380, Tech Brief, Intersil Corporation, Choosing the IF Frequency for the PRISM II 11 MBPS Radio Reference Design

Intersil documents can be found on the Premier Web site.

## Appendix A  Synthesizer Phase Noise/Jitter Analysis

### TABLE 4. PRISM 2.5 LO PHASE NOISE ANALYSIS

<table>
<thead>
<tr>
<th>FREQ OFFSET</th>
<th>dBc/Hz</th>
<th>NOTES</th>
<th>PHASE JITTER (RADIANS Squared)</th>
<th>PHASE JITTER (RMS DEGREES)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10K</td>
<td>-91.5</td>
<td>1.059E-05</td>
<td>0.186</td>
<td></td>
</tr>
<tr>
<td>20K</td>
<td>-98.1</td>
<td>4.635E-06</td>
<td>0.123</td>
<td></td>
</tr>
<tr>
<td>50K</td>
<td>-108</td>
<td>1.423E-06</td>
<td>0.068</td>
<td></td>
</tr>
<tr>
<td>100K</td>
<td>-113</td>
<td>7.504E-07</td>
<td>0.050</td>
<td></td>
</tr>
<tr>
<td>200K</td>
<td>-114.5</td>
<td>1.062E-06</td>
<td>0.059</td>
<td></td>
</tr>
<tr>
<td>500K</td>
<td>-122</td>
<td>5.665E-07</td>
<td>0.043</td>
<td></td>
</tr>
<tr>
<td>1000K</td>
<td>-123</td>
<td>1.750E-06</td>
<td>0.076</td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>2.078E-05</td>
<td>0.261</td>
<td></td>
</tr>
</tbody>
</table>

### 748MHz LO MEASURED PERFORMANCE

<table>
<thead>
<tr>
<th>FREQ OFFSET</th>
<th>dBc/Hz</th>
<th>NOTES</th>
<th>PHASE JITTER (RADIANS Squared)</th>
<th>PHASE JITTER (RMS DEGREES)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10K</td>
<td>-88.8</td>
<td>1.973E-05</td>
<td>0.254</td>
<td></td>
</tr>
<tr>
<td>20K</td>
<td>-93.8</td>
<td>1.248E-05</td>
<td>0.202</td>
<td></td>
</tr>
<tr>
<td>50K</td>
<td>-97.3</td>
<td>1.672E-05</td>
<td>0.234</td>
<td></td>
</tr>
<tr>
<td>100K</td>
<td>-99.5</td>
<td>1.679E-05</td>
<td>0.235</td>
<td></td>
</tr>
<tr>
<td>200K</td>
<td>-102</td>
<td>1.888E-05</td>
<td>0.249</td>
<td></td>
</tr>
<tr>
<td>500K</td>
<td>-103.3</td>
<td>4.200E-05</td>
<td>0.371</td>
<td></td>
</tr>
<tr>
<td>1000K</td>
<td>-102.5</td>
<td>1.964E-04</td>
<td>0.803</td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>3.229E-04</td>
<td>1.030</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** Assume worst case, RMS measured 2.1GHz and 748MHz LO

<table>
<thead>
<tr>
<th>LO Frequency</th>
<th>PHASE JITTER (RADIANS Squared)</th>
<th>PHASE JITTER (RMS DEGREES)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.063GHz LO</td>
<td>2.078E-05</td>
<td>0.261</td>
</tr>
<tr>
<td>748MHz LO</td>
<td>3.229E-04</td>
<td>1.030</td>
</tr>
<tr>
<td>Total</td>
<td>3.437E-04</td>
<td>1.291</td>
</tr>
</tbody>
</table>
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