The goal of this exercise is to design and simulate a CMOS OpAmp suitable for use as a buffer for a voltage scaling D/A converter. The design is to be undertaken in a standard 0.18µm N-well process (i.e., no twin well structures available).

The D/A converter is assumed to have an input range from 0.3V to 0.8V, and the buffer is required to have a gain of X1 to give a final output from 0.3V to 0.8V.

The specifications for load and maximum operating frequency are given with respect to your student ID number in the table below.

The dynamic performance of the OpAmp must be suitable for full scale sinusoidal outputs up to the specified frequency. The load for the buffer is any parallel combination of resistance greater than the specified value of $R_L$, and capacitance less than the specified value of $C_L$.

The OpAmp should be stable for any combination of these. Since the output is supplied from a D/A converter, the step response of the amplifier in the target application must be well controlled for any specified load, and with a step input within the range 0.3V - 0.8V should settle to within 1% of the final value within a time of less than $\tau_s$ with less than 15% overshoot.

The specifications are as follows:

**Power Supply**
- 1.8V single supply with respect to ground

**Application Mode Gain and Output Range**
- For use in x1 non-inverting mode with input in the range 0.3V - 0.8V, and output in the range 0.3V – 0.8V

**Sinusoidal Input Test Signal and Range**
- 0.25V peak, common mode level 0.55V. Frequency as per table below.

**Step Input Test Signal and Range**
- 0.3V – 0.8V, in 0.1V steps up to full range with 1ns rise/fall time at input

**Output Load Conditions**
- (i) capacitor in the range from 0pF up to $C_L$ pF referred to ground
- and, for extended specification only, in parallel with
- (ii) resistor from $R_L$ Ω up to open circuit conditions, again referred to ground

**Open Loop DC Gain**
- Greater than 60dB (with all specified loads), Achieved over input common mode range from 0.3V – 0.8V, output range from 0.3V – 0.8V

**Full Power Bandwidth**
- Greater than specified $f_{\text{max}}$ at 0.5V p-p output with all specified loads
Small Signal Bandwidth
   The amplifier should have an open loop gain of more than 26dB at the full power test
   frequency (this will set the Unity Gain Frequency).

Phase Margin
   Better than 45deg in open loop conditions with specified load

Settling
   Settling to within 1% of final value within $\tau_s$ with less than 15% overshoot over all valid
   input and output signal range with all specified load conditions.

Bias
   The amplifier may be biased from an ideal 25uA source (you may connect this to whichever
   supply rail you choose).

Basic Assignment Goals (up to 80% marks achievable)

Prepare a report on the design, not more than 15 pages including simulation results, including the
following:

1. Hand calculations, with a brief explanation of how the specification is to be met
2. SPICE simulation results of:
   (a) Small signal Gain and Phase at various common mode DC levels at min max and
       median input and output levels over the specified ranges (0.3V – 0.8V in, 0.3V – 0.8V
       out) with specified range of load capacitance (i.e., min, max and geometric mean value),
       showing gain and phase margins
   (b) DC transfer characteristic, showing output range of acceptable gain and any offset
   (c) Step (transient) response with staircase input (using summation of pulse sources
       as shown) showing the settling time as a function of common mode input and output
   (d) Full amplitude sine wave transient simulation with 0.25V peak sine with 0.55V DC
       common mode input and specified loads.

Tasks for the extended assignment (for 100% marks):

(e) For the simulations (a) to (d) above, meet the settling and full power bandwidth
   requirements with a parallel load resistance to ground $R_L$, and show that the open loop
   gain is maintained greater than 55dB for all output DC voltages from 0.3V up to 0.8V.

Test Frequency, Settling Time and Load Conditions

The full power test frequency, load conditions and step input settling time are to be taken
depending on your student ID number.

<table>
<thead>
<tr>
<th>Student ID ending in</th>
<th>Pull Power Test Frequency</th>
<th>Settling Time $\tau_s$</th>
<th>$C_L$ (max)</th>
<th>$R_L$ (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0, 1, 2</td>
<td>50kHz</td>
<td>2.5µs</td>
<td>200pF</td>
<td>2kΩ</td>
</tr>
<tr>
<td>3, 4, 5</td>
<td>100kHz</td>
<td>1.2µs</td>
<td>120pF</td>
<td>2.5kΩ</td>
</tr>
<tr>
<td>6, 7, 8, 9</td>
<td>200kHz</td>
<td>0.7µs</td>
<td>55pF</td>
<td>3kΩ</td>
</tr>
</tbody>
</table>
Simulation testing arrangements ("test benches") are shown below.

**D/A BUFFER APPLICATION CIRCUIT**

**OP-AMP BASIC AC (Small Signal) GAIN/PHASE SIMULATION TEST SET-UP**

Vin: AC - Use AC value of 1V for small signal simulations

VinCM: Put DC source in series to set common mode of input i.e., 0.3V to 0.8V
OP-AMP LARGE SIGNAL SINE FULL POWER BANDWIDTH SIMULATION TEST SET-UP

VIN:
Sine 0.25V pk at Specified Full Power Test Freq, and also 1/10 and 10X of this Frequency

VINCM:
Put DC source in series to set common mode of input at 0.55V

OP-AMP LARGE SIGNAL STEP RESPONSE SIMULATION TEST SET-UP

V1-5 Pulse sources. Each 1ns rise time, 0V - 0.1V step, Time between edges when added = 2.5us

Vmin DC value 0.3V
Ensure that the simulations and plots have sufficient resolution to demonstrate that the specifications have indeed been met. Don’t interpolate results across a very few numbers. **To make the plots more readable, please change the plot options so that the background is white** (the default in LTSPICE is black)

It is helpful to include edited sections of the input netlist, plotted results, and some numerical output values for critical points (e.g. unity gain frequency).

**Some Guidance:**

There are many possible circuits that can meet the specifications.

When doing the hand calculations bear in mind that the device parameters in the table below are for very simplified modelling, and real devices behave in more complicated ways. So expect to do some optimisation with SPICE, but explain what you have done in your report.

Device saturation is not an abrupt transition, particularly as geometry gets smaller, and the output resistance continues to rise as VDS increases above the saturation voltage given by simple theory, until it reaches a more idealised limit. This will be evident when looking at the gain vs the common mode levels, and in biasing cascode circuits.

Device threshold values will also show some variation with channel length.

Do not be constrained by any particular channel length of transistor - remember that longer channel devices can be useful in obtaining good LF gain. Do not go too far with this, as there will come a point when it may incur bandwidth and settling penalties.

To view the operating conditions of the devices with static bias, use the operating point simulation (.OP command) and then view the SPICE ERROR LOG file. This shows all the small signal parameters of the devices used.

It is good practice to create a special symbol for the amplifier and put it in the test circuits. If you do this, it creates a subcircuit in SPICE, and you need to save the subcircuit device currents and voltages, by using the selectable option in the SPICE control panel.

Remember that you may need to invoke the NODESET option of SPICE in order to obtain DC convergence - this involves having hand calculated node voltages available to force the simulator to converge.
Because of the resistive load, a two stage design is probably needed. The values of $V_{gs}-V_t$ at the output and input need to be such that you can meet the signal range. Try to avoid going below 150mV as the simple calculations will not work at well.

Do not be constrained by any particular channel length of transistor - remember that longer channel devices can be useful in obtaining good LF gain, and if you use a relatively simple amplifier design, you will probably need to use longer transistors. Don’t go too far with this strategy, as it may cause bandwidth problems.

For the extended assignment specifications, the resistive load will reduce the gain of any output stage, and so you will need to make up the gain in another stage.

### HAND CALCULATION PROCESS PARAMETERS FOR ASSIGNMENT

$(L_{min} = 0.18\mu m, V_{dd \ max} = 1.8V + 10\%$. NB: These are only a guide at a typical bias, simulation results may differ depending on device sizes and bias)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>N</th>
<th>P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\mu C_{ox}$</td>
<td>330</td>
<td>100</td>
<td>$\mu A/V^2$</td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>8.2</td>
<td>8.2</td>
<td>fF/$\mu^2$</td>
</tr>
<tr>
<td>$n \ (at \ V_{BS} = 0)$</td>
<td>1.3</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>$\theta$</td>
<td>0.3</td>
<td>0.3</td>
<td>V$^{-1}$</td>
</tr>
<tr>
<td>$\varepsilon C$</td>
<td>0.17</td>
<td>0.04</td>
<td>V/m</td>
</tr>
<tr>
<td>$C_{GD0}$</td>
<td>700</td>
<td>700</td>
<td>aF/μ</td>
</tr>
<tr>
<td>$C_{GS0}$</td>
<td>700</td>
<td>700</td>
<td>aF/μ</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.033/(L – 0.03)</td>
<td>0.033/(L – 0.03)</td>
<td>V$^{-1}$</td>
</tr>
<tr>
<td>$V_{TO}$</td>
<td>0.44</td>
<td>0.47</td>
<td>V</td>
</tr>
<tr>
<td>$C_{DB}$</td>
<td>1.2</td>
<td>1.2</td>
<td>fF/$\mu^2$</td>
</tr>
<tr>
<td>$C_{SB}$</td>
<td>1.2</td>
<td>1.2</td>
<td>fF/$\mu^2$</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>0.53</td>
<td>0.6</td>
<td>V$^{1/2}$</td>
</tr>
<tr>
<td>$\Phi_B$</td>
<td>0.7</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>$A_{VT}$</td>
<td>0.006</td>
<td>0.005</td>
<td>V$\mu$m</td>
</tr>
<tr>
<td>$A_\beta$</td>
<td>0.010</td>
<td>0.009</td>
<td>μm</td>
</tr>
</tbody>
</table>
Simulation CAD

The recommended simulation tool is LTSpice, available as a download from Linear Technology Inc at the following link:

http://www.linear.com/designtools/software/switchercad.jsp

When drawing the schematics remember to

- use the 4 terminal MOS symbols, found in the LTSpice library as nmos4 and pmos4.
- make sure the substrate connections are correct for an N-Well CMOS process
- assign the models (CMOS18N and CMOS18P) to the instances and put in the device width and length values.
- use the form \( w=10u \) to show that MOS dimensions are in microns

The parameters used in SPICE are for a BSIM 3 model, and as such, do not correspond (at all!) to the simple Schichman-Hodges model given for hand analysis.

SPICE models for the technology are based on the BSIM 3 model, and should be included in the simulation by putting a reference to the model file (with a name yourmodels.lib) on the schematic by means of the .INCLUDE function.

The file is available to copy/paste from the ELEC6232 notes intranet page. Note that this file also contains 0.35um models corresponding to thick gate oxide devices. Do not use the 0.35um models in this design.

For reference the models are as follows:

```
************************************************************
* THIN GATE OXIDE "CORE" CMOS Transistors, L Min = 0.18 um *
************************************************************

.MOD CMOS18N NMOS (LEVEL   = 8
+VERSION = 3.1          TNOM   = 27          TOX    = 4.2E-9
+XJ     = 1E-7          NCH    = 2.3549E17     VTH0   = 0.3515862
+K1     = 0.5738018     K2     = 3.556293E-3   K3     = 2.4714554
+K3B    = -10           W0     = 5.453803E-6   NLX    = 1.877957E-7
+DVT0W   = 0            DVT1W   = 0            DVT2W   = 0
+dDVT0   = 1.6002255    dDVT1   = 0.4265843    dDVT2   = 0.0245845
+U0     = 321.376422   UA     = -2.23416E-11  UB     = 2.599723E-19
+UC     = -6.75545E-11  VSAT   = 8.796503E4   A0     = 1.5315135
+AGS    = 0.2109775     B0     = -1.399509E-8  B1     = -1E-7
+KETA   = 0.0233539     A1     = 0            A2     = 1
+rDWSW   = 148.8082664  PRWG   = 0.5          PRWB   = -0.2
+WR     = 1            WINT   = 0            LINT   = 1.373066E-8
+XL     = -2E-8        XW     = -1E-8        DWG    = 7.415312E-9
+dWDB    = -5.829809E-9 VOFF   = -0.0609863  NFACTOR = 2.4645328
+CID    = 0            CDSC   = 2.4E-4        CDSCD   = 0
+CDSCB  = 0            ETA0   = 0.0125069     ETAB   = -0.0388032
+DSUB   = 0.8868103    PCLM   = 0.7773539    PDIBLC1 = 0.0820772
```

---

7
+PDIBLC2 = 0.01   PDIBLCB = -0.1   DROUT = 0.5443127
+PSCEB1 = 7.979323E10  PSCEB2 = 1.522921E-9   PVAG = 0
+DELT A = 0.01   RSH = 6.5   MOBMOD = 1
+PRT = 0   UTE = -1.5   KT1 = -0.11
+KTIL = 0   KT2 = 0.022   UA1 = 4.31E-9
+UB1 = -7.61E-18   UC1 = -5.6E-11   AT = 3.3E4
+WL = 0   WL N = 1   WW = 0
+WNN = 1   WL WL = 0   LL = 0
+LLN = 1   LW = 0   LWN = 1
+LWL = 0   CAPMOD = 2   XPAR T = 0.5
+CGDO = 7.72E-10   CGSO = 7.72E-10   CGBO = 1E-12
+CJ = 9.85195E-4   PB = 0.7385615  MJ = 0.3655087
+CJSW = 2.406794E-10  PB SW = 0.92385   MJ SW = 0.1270086
+CF = 0   PVTH0 = 1.170057E-4  PRDSW = -3.6480357
+PK2 = -4.174409E-4   WK ETA = -2.170673E-3   LK ETA = -7.428932E-3
+PU0 = 6.7215458   PUA = 1.026946E-11  PUB = 0
+PVSAT = 1.627385E3   PETA0 = 1E-4   PK ETA = 1.451175E-3
.*

.MODEL CMOS18P PMOS (LEVEL = 8
+VERSION = 3.1   TNOM = 27   TOX = 4.2E-9
+XJ = 1E-7   NCH = 4.1589E17  VTH0 = -0.4175952
+K1 = 0.5750296  K2 = 0.0307468  K3 = 0
+K3B = 4.0114633  W0 = 1E-6   NLX = 9.1517E-8
+DVT0W = 0   DVT1W = 0   DVT2W = 0
+DVT0 = 0.46178   DVT1 = 0.2538901  DVT2 = 0.1
+U0 = 124.7137948  UA = 1.725572E-9  UB = 1E-21
+UC = -1E-10   VSAT = 1.459962E5   A0 = 1.5412231
+AGS = 0.3606062  B0 = 1.658511E-6   B1 = 5E-6
+KETA = 0.0232949  A1 = 0.060828  A2 = 0.9998877
+RDSW = 243.2475193  PRWG = 0.5   PRWB = -0.5
+WR = 1   WINT = 2.184965E-10  LINT = 2.241244E-8
+XL = -2E-8   XV = -1E-8   DWG = 1.671645E-8
+DBW = 7.750596E-9   VOFF = -0.0970621  NFAC TOR = 1.9534869
+CI T = 0   CDSC = 2.4E-4   CDSCD = 0
+CDSCB = 0   ETA0 = 0.0561272  ETAB = -0.0691133
+DSUB = 0.723934   PCLM = 2.6509807   PDIBLC1 = 1.248878E-7
+PDIBLC2 = 0.0746228   PDIBLCB = -1E-3   DROUT = 0
+PSCEB1 = 1.733994E9  PSCEB2 = 5.003177E-10  PVAG = 15
+DELT A = 0.01   RSH = 7.2   MOBMOD = 1
+PRT = 0   UTE = -1.5   KT1 = -0.11
+KTIL = 0   KT2 = 0.022   UA1 = 4.31E-9
+UB1 = -7.61E-18   UC1 = -5.6E-11   AT = 3.3E4
+WL = 0   WL N = 1   WW = 0
+WNN = 1   WL WL = 0   LL = 0
+LLN = 1   LW = 0   LWN = 1
+LWL = 0   CAPMOD = 2   XPAR T = 0.5
+CGDO = 6.92E-10   CGSO = 6.92E-10  CGBO = 1E-12
+CJ = 1.197687E-3   PB = 0.825066  MJ = 0.3990899
+CJSW = 1.795391E-10  PB SW = 0.5788985  MJ SW = 0.2726342
+CJSW G = 4.22E-10   PB SWG = 0.5788985  MJ SWG = 0.2726342
+CF = 0   PVTH0 = 2.971199E-3  PRDSW = 5.2868005
+PK2 = 2.575607E-3   WK ETA = 2.432366E-3   LK ETA = -4.477373E-4
+PU0 = -2.3488719   PUA = -7.80433E-11  PUB = 1.421649E-24
+PVSAT = -50   PETA0 = 1E-4   PK ETA = 6.128011E-4
*