Microprocessors in embedded systems

- Microprocessors are everywhere
- A modern car has around 40 to 100 microprocessors
  - Engine control, brake systems, active suspension
    - Need powerful, 32-bit processors
  - Even motorised window control has a microprocessor

An embedded system:
- A system that utilizes custom hardware and software to carry out specific tasks

Embedded Hardware:
- Microprocessor
- Application-specific hardware generally used for accelerating time-critical tasks

Embedded software running on the microprocessor:
- Almost every modern embedded system contains at least one microprocessor
- Designers face many challenges
  - Which parts of a system on chip should be implemented as programmable, combinational and sequential logic?
  - Which parts should be implemented as programs on a microprocessor core?
  - What processor architectures should be used?
    - Little point in using a 32-bit MIPS with double precision floating point if one is designing a burglar alarm
Core-based embedded system design

- Designers re-use pre-designed hardware components called “Intellectual Property (IP) Cores”
- This approach reduces design time at the expense of performance, area etc
- Soft-core embedded processors – Complete microprocessors described in a hardware description language (SystemVerilog, Verilog, VHDL) that can be customised for specific tasks

‘Hard’ Processor Cores

- A hard core processor is an embedded dedicated processor, e.g. ARM
  - On an FPGA it is surrounded by FPGA’s memory and programmable logic
  - On an ASIC, a ‘hard’ core is surrounded by custom logic
- The picoMIPS you are designing is a soft core.
- Hard cores are less configurable but have higher performance than soft cores

Hard processor cores

Altera offers ARM cores in some of their FPGAs, e.g. Cyclone V:

Hard processor cores - cont

Xilinx also offers ARM or PowerPC

Two PowerPC hard cores on a Xilinx Virtex II die
Advantages of soft cores

- Higher level of abstraction – easier to understand
- More flexible – designers can change the core by editing source code or selecting parameters (more on that later)
- Platform independent – can be synthesized for any IC technology, including FPGAs, ASICs, etc.
- More immune to obsolescence

Examples of soft cores

- Altera: NIOS II – one of the most popular
- Xilinx: MicroBlaze, PicoBlaze
- Lattice: LatticeMico8
- ARM Cortex M1
  – a third party core offered to FPGA vendors
- There are many open source soft cores, e.g.
  – SPARC - GPL licence, (e.g. www.simplyrisc.com)
  – OpenRISC – also GPL (e.g opencores.org)
  – DSPuva16 – from University of Valladolid, Spain

Soft cores

- Use existing FPGA logic elements
- Flexible, feature rich, reconfigurable
- Customized memory size, data path width, ALU functionality, number and types of peripherals
- Typically have slower clock rates
- Are said to consume more power than their hard-core counterparts
  – Nb. I doubt if this is always true
Development tools

- A dedicated CAD tool, specific to the particular core, is used to specify processor parameters
  - Register file size, hardware arithmetic, floating point, interrupts, I/O hardware, custom functions
  - User programs, typically written in C or C++, are compiled by a custom compiler provided by the CAD tool and included in the synthesis
- The tool outputs a synthesizable HDL model
  - Normally the HDL code is protected and not viewable
- After any user-specified hardware is added, the design is synthesised using a standard synthesis tool
  - NB. Altera Quartus integrates specification for the NIOS processor into a single tool used for general purpose synthesis
  - Altera also provide a SOPC (System on Programmable Chip) Builder for advanced embedded system design

Alter Nios II Soft Core Processor

- A general purpose RISC with a Harvard memory architecture.
- Features a 32-bit Instruction Set Architecture (ISA), 32 general-purpose registers, single-instruction 32x32 multiply and divide operations, and dedicated instructions for 64-bit and 128-bit products of multiplication.
- Nios II has a performance of more than 150 Dhrystone MIPS (DMIPS) on Stratix family of FPGAs.
- Comes in three versions: economy, standard and fast core.
- Each core version has a different number of pipeline stages, instruction and data cache memories and hardware components for multiply and divide operations.
- Each core implementation varies in size and performance depending on the features that are selected.
- Adding peripherals with the Nios II Processors is done through the Avalon Interface Bus which contains the necessary logic to interface the processor with off-the-shelf IP cores or custom designed peripherals.

source: Tong J.G e.a. “Soft core processors for embedded systems”, 18th Int Conf on Microelectronics (ICM), 2006

Comparison of some soft core processors

<table>
<thead>
<tr>
<th>Category</th>
<th>Nios II (Fast Core)</th>
<th>Microblaze</th>
<th>Virtex 6</th>
<th>OpenRISC 1200</th>
<th>LEON3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum MIPS</td>
<td>150 (32-bit)</td>
<td>50 (32-bit)</td>
<td>100 (32-bit)</td>
<td>1200 (32-bit)</td>
<td>1200 (32-bit)</td>
</tr>
<tr>
<td>ADL/FFP IC Technology</td>
<td>Stratix IV</td>
<td>Stratix IV</td>
<td>Stratix IV</td>
<td>Stratix IV</td>
<td>Stratix IV</td>
</tr>
<tr>
<td>Reported DMIPS</td>
<td>130 DMIPS</td>
<td>120 DMIPS</td>
<td>120 DMIPS</td>
<td>120 DMIPS</td>
<td>120 DMIPS</td>
</tr>
<tr>
<td>Cycle Count (MHz)</td>
<td>125 MHz</td>
<td>50 MHz</td>
<td>250 MHz</td>
<td>125 MHz</td>
<td>125 MHz</td>
</tr>
<tr>
<td>Floating Point (multiply)</td>
<td>32-bit</td>
<td>32-bit</td>
<td>32-bit</td>
<td>32-bit</td>
<td>32-bit</td>
</tr>
<tr>
<td>Pipeline Stages</td>
<td>4 Stages</td>
<td>4 Stages</td>
<td>4 Stages</td>
<td>4 Stages</td>
<td>4 Stages</td>
</tr>
<tr>
<td>Cache Size</td>
<td>Up to 256 Kbytes</td>
<td>16 Kbytes</td>
<td>256 Kbytes</td>
<td>256 Kbytes</td>
<td>256 Kbytes</td>
</tr>
<tr>
<td>Register File Size</td>
<td>32 R registers</td>
<td>32 R registers</td>
<td>32 R registers</td>
<td>32 R registers</td>
<td>32 R registers</td>
</tr>
<tr>
<td>Technology</td>
<td>FPGA</td>
<td>FPGA</td>
<td>FPGA</td>
<td>FPGA</td>
<td>FPGA</td>
</tr>
<tr>
<td>Area</td>
<td>700,168 LUTs</td>
<td>128 K LUTs</td>
<td>256 K LUTs</td>
<td>256 K LUTs</td>
<td>256 K LUTs</td>
</tr>
</tbody>
</table>
source: altera.com
**NIOS II Scalability**

- Low-Cost Embedded Solution
- Complex Embedded System-on-a-Chip

**Processor?**
- Cyclone Series & Nios II Economy
  - CPU < 20% of Device
  - 20 DMIPS
  - As Low as 15€

**How Many Processors?**
- 179,400 Logic Elements

**Stratix II EP2S180 & Nios II Fast**
- CPU 1% of Device

source: altera.com

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**NIOS II Scalability – cont.**

- 32-Bit Pipelined RISC Architecture
  - 16-Bit Instructions
  - Most Instructions Take 1 Clock
- Large Internal Register File
- Configurable Data Path
  - 16-bit (1400 LEs)
  - 32-bit (1700 LEs)
- Dynamic Bus Sizing
- 30 to 80 MIPS Performance

source: altera.com

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**NIOS II cache and RAM performance**

<table>
<thead>
<tr>
<th>Memory</th>
<th>I-Cache</th>
<th>D-Cache</th>
<th>Normalised Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDRAM</td>
<td>No</td>
<td>No</td>
<td>40.2%</td>
</tr>
<tr>
<td>SDRAM</td>
<td>No</td>
<td>Yes</td>
<td>55.2%</td>
</tr>
<tr>
<td>SDRAM</td>
<td>Yes</td>
<td>No</td>
<td>64.3%</td>
</tr>
<tr>
<td>SDRAM</td>
<td>Yes</td>
<td>Yes</td>
<td>96.4%</td>
</tr>
<tr>
<td>OnChip</td>
<td>No</td>
<td>No</td>
<td>100.0%</td>
</tr>
<tr>
<td>OnChip</td>
<td>No</td>
<td>Yes</td>
<td>98.0%</td>
</tr>
<tr>
<td>OnChip</td>
<td>Yes</td>
<td>No</td>
<td>110.2%</td>
</tr>
<tr>
<td>OnChip</td>
<td>Yes</td>
<td>Yes</td>
<td>105.6%</td>
</tr>
</tbody>
</table>

Performance relative to on chip RAM with no Cache running dhrystone modified for unbuffered I/O

source: altera.com

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**NIOS II windowed register file**

- Common Technique Used by High-Performance CPUs
  - Provides Fast Subroutine Calls
- Up to 512 General-Purpose Registers
- Movable Window With Access to 32 Registers
  - 24 Register Window (Movable)
  - 8 Global Registers (Fixed)
- Automatically Used by C Compiler

source: altera.com
NIOS II Multiplier option

- **MSTEP** – hardware option 1
  - Sequential, one-bit per clock,
  - cheap but less performance
- **MUL** – hardware option 2
  - Combinational, 16x16-bit multiplication in 2 clocks

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>Additional Logic Elements Used</th>
<th>16x16=32</th>
<th>32x32=32</th>
</tr>
</thead>
<tbody>
<tr>
<td>None (Software)</td>
<td>0</td>
<td>80</td>
<td>250</td>
</tr>
<tr>
<td>MSTEP</td>
<td>+200</td>
<td>18</td>
<td>80</td>
</tr>
<tr>
<td>MUL</td>
<td>+400</td>
<td>2</td>
<td>16</td>
</tr>
</tbody>
</table>

source: altera.com

NIOS II System Builder

Typical applications of NIOS

- Many Altera recommended standard HDL modules for Altera FPGA development systems are based on NIOS, e.g.
  - USB port
  - Ethernet
  - UART
  - Parallel I/O port
  - SPI (Serial Peripheral Interface) ports
  - Timers

NIOS II application example: Ethernet controller

- 10/100-Mbps SMSC LAN91C111 single-chip Ethernet controller interface
- Software support provided by the NicheStack TCP/IP Stack - Nios II Edition
- Included with the Nios II development kits

source: altera.com
Open source soft cores

- There are a great number of soft-cores freely available from open-source communities and commercial vendors
- Some examples
  - LEON by Gaisler Research
  - OpenRISC 1200 from opencores.org
  - RISC V from riscv.org
  - Ensilica, both open and commercial cores, www.ensilica.com
    - Some Ensilica open source projects:
      - FT816Float - Floating point accelerator
      - Versatile FIFO
      - SPI Verilog Master & Slave modules
      - AVR Core

Summary

- Popularity of embedded soft-core and hard-core processors increases
  - It is difficult to imagine a complex system-on-chip design without at least one embedded processor core
- Most popular embedded processors use RISC/Harvard architectures
- ARM Cortex seems to be the most popular hard core
- Altera NIOS II – most popular soft core
- Some good videos on youtube:
  - An Altera man explains NIOS: http://www.youtube.com/watch?v=GbG0NyQ1zrU
  - Another Altera man advocates soft MIPS: http://www.youtube.com/watch?feature=player_embedded&v=TWWS3ckl-Kw
  - A student demonstrates his dual core soft MIPS on FPGA: http://www.youtube.com/watch?v=i9TNNvVhVks, see also: www.realmib.com/portfolio/