Example Sheet 1

1. Write a SystemVerilog model for the function $Z = A \cdot B + C \cdot D$.

2. A comparator is used to determine whether two signals have equal values. A one-bit comparator is described by

$$eqo = \neg(x \oplus y) \& eqi;$$

where $eqi$ is the result of the comparison of other bits and $eqo$ is passed to the next comparison operation. Write a model of a 4-bit iterative comparator.