1. Write a behavioural SystemVerilog model of a negative edge triggered D flip-flop with set and clear.
2. Write a SystemVerilog model of a negative edge-triggered T-type flip-flop.
3. Write a SystemVerilog model of a 10-state synchronous counter that asserts an output when the count reaches 10.
4. Write a SystemVerilog model of an N-bit counter with a control input “Up”. When the control input is ‘1’ the counter counts up; when it is ‘0’ the counter counts down. The counter should not, however, wrap round. When the all ‘1’s or all `0's states are reached the counter should stop.
5. Write a SystemVerilog model of an N-bit parallel to serial converter.
6. Design a counter which cycles through the following states:
   001,010,101,011,111,110,100

Write testbenches for all your answers.
Verify your designs by simulation.