IEEE1500 Architecture
**System Chip with Wrapped Cores**

- **TAM Source/Sink**
  - From chip I/O, test bus/rail/port, BIST, etc...

- **TAM In/Out**
  - 0 to n lines for parallel and/or serial test data, or test control

- **Wrapper Interface Port (WIP)**
  - From chip-level TAP Controller, chip I/O, ...
IEEE1500 Architecture Components

- IEEE1500 Wrapper:
  - WIR for loading wrapper instructions
  - WBR with Wrapper Cells at each terminal
  - A Bypass register for the SII
  - WIP for control of Wrapper Registers via SII
    - May also provide controls for PI/TAM

Wrapper Cells form the Wrapper Boundary Register (WBR)
Wrapper Instruction Register (WIR)
Wrapper Serial Input (WSI)
Wrapper Interface Port (WIP)
Wrapper Serial Output (WSO)
Wrapper Bypass Register
TAM-In TAM-Out
The Wrapper Bypass Register provides a scan bypass from WSI to WSO.

- WIP selects the WIR or a Wrapper Data Register (WDR) between WSI and WSO.
- Updated WIR output determines:
  - Which WDR (i.e. Bypass, CDR, or WBR) is selected between WSI and WSO.
  - The current P1500 Wrapper Mode and (optionally) the Core Mode.
  - If a user defined TAM connection & register configuration is enabled.
Wrapper Interface Port (WIP)

WIP Signals for Accessing WIR, Bypass & WDRs

- WRSTN
- TransferDR
- UpdateWR
- ShiftWR
- CaptureWR
- SelectWIR
- WRCK
- WSI

The WIP is used to access the WIR, Bypass & other data registers via the S11.

WIP Terminals:

- WRCK is the wrapper clock
  - Dedicated for WIR and BYPASS, WBR may also use "auxiliary" clock(s)
- WRSTN is an asynchronous Wrapper Reset
- SelectWIR selects whether the WIR or DR(s) is connected between WSI and WSO
- UpdateWR, ShiftWR and CaptureWR are enables for register operations
  - May be used for gating WRCK clock internal to Wrapper
Wrapper Boundary Cells

Wrapper Boundary Cells are required on all functional core terminals.

Wrapper Boundary Cells are not required on Test terminals or "Special Case" terminals, such as analog.
**Wrapper Boundary Cells**

**Overview of Cell Modes**

- **D Cell Modes**
  - **Normal**: No Effect, core functions normally
  - **Inward Facing**: Affects the core, test is directed towards core
  - **Outward Facing**: Affects the core, test is directed outward from core
  - **Safe**: Affects the core & ensures wrapper does not damage core or system (a recommended mode)
Wrapper Boundary Cells
Overview of Cell Events

D Cell Events
- **Shift**: Move data through shift path
- **Capture**: Sample data
- **Apply**: Moment when test data becomes active and effective
- **Update**: 1149.1-type Update
- **Transfer**: Move data from Update element to Shift path
Wrapper Boundary Cells
Overview of Cell Types

1149.1 Type Cell Example

D Cell Modes
- Normal
- Inward Facing
- Outward Facing
- Safe

D Cell Events
- Shift
- Capture
- Apply
- Update
**P1500 Architecture**

Wrapper Example: TAM Coupled to Core Logic via PIL

- Core internal scan paths & WBR are connected in parallel to TAM by a "Core Test" instruction.
- Today, many flavors of "TAMs" & TAM "Interfaces" exist.