CMOS logic circuits

ELEC 1202

How do we connect FETs?
Comparing market sizes and forecasted growth rates for systems ICs.

[Graph: Total Memory IC Market ($B)]

Source: IC Insights

[Graph: End-Use Systems Markets ($B) and Growth Rates]

[Link: http://eecatalog.com/chipdesign/2015/03/18/comparing-market-sizes-and-forecasted-growth-rates-for-systems-ics/]

Basis of NMOS Inverter

- Drain current $i_D$
- $V_{DD}$ positive power supply
- Load resistor $R_L$
- Gate-source voltage $V_{GS}$
- Drain-source voltage $V_{DS}$
- $0V$
Inverter circuits

NMOS

PMOS

PMOS
# CMOS inverter

<table>
<thead>
<tr>
<th>Input</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>‘0’</td>
<td>OFF</td>
<td>ON</td>
<td>‘1’</td>
</tr>
<tr>
<td>‘1’</td>
<td>ON</td>
<td>OFF</td>
<td>‘0’</td>
</tr>
</tbody>
</table>

![CMOS inverter diagram](image)
## CMOS NAND

<table>
<thead>
<tr>
<th>Input $A$</th>
<th>Input $B$</th>
<th>P1</th>
<th>P2</th>
<th>N1</th>
<th>N2</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>‘0’</td>
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CMOS NAND

The physical layout of a NAND circuit. The larger regions of N-type diffusion and P-type diffusion are part of the transistors. The two smaller regions on the left are taps to prevent latchup.

https://en.wikipedia.org/wiki/CMOS
Advantages of CMOS

The main advantage of MOS technology is that it has very low power consumption.