ELEC 2221 Digital Systems and Signal Processing

Complex Programmable Logic Devices (CPLD)

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Session Outline

- PLA
- PAL
- CPLD
- MACH XO
Types of PLDs

Equivalent logic gates

- Xilinx Virtex UltraScale, eq. 50mn ASIC gates
- Altera Stratix V, eq. 15mn ASIC gates
- Xilinx Virtex-6
- Altera Cyclone IV
- Lattice MachXO
- Altera MAX 9000
- Lattice ispGAL 22v10

PLD | CPLD | FPGA
Three major types of PLDs

- **SPLD (Simple Programmable Logic Devices)**
  - Typically equivalent to a few hundred of logic gates
  - Fixed internal routing (PAL or PLA)

- **CPLD (Complex Programmable Logic Devices)**
  - Multiple SPLDs on a single chip
  - Programmable routing

- **FPGA (Field Programmable Logic Devices)**
  - An array of logic blocks
  - Equivalent to up to 1mln logic gates
Simple PLDs

- PLA – programmable logic array
  - Logic functions realised in sum-of-product form
  - Both AND and OR arrays programmable
- PAL – programmable array logic
  - Proprietary PLDs introduced by AMD in 1980s
  - Only AND array is programmable (less expensive, better performance)
  - Became inexpensive and popular in 1990s due to electrically-erasable CMOS implementation
Programmable Logic Array (PLA)

- Use to implement circuits in SOP form
- The connections in the AND plane are programmable
- The connections in the OR plane are programmable
Gate Level of PLA

\[ f_1 = x_1 x_2 + x_1 x_3' + x_1' x_2 x_3 \]
\[ f_2 = x_1 x_2 + x_1' x_2' x_3 + x_1 x_3 \]
Customary Schematic of a PLA

\[ f_1 = x_1 x_2 + x_1 x_3' + x_1' x_2' x_3 \]
\[ f_2 = x_1 x_2 + x_1' x_2' x_3 + x_1 x_3 \]

x marks the connections left in place after programming

AND plane

OR plane

P₁
P₂
P₃
P₄

\( f_1 \)
\( f_2 \)
Limitations of PLAs

PLAs come in various sizes

- Typical size is 16 inputs, 32 product terms, 8 outputs
  - Each AND gate has large fan-in → this limits the number of inputs that can be provided in a PLA
  - 16 inputs → $3^{16}$ = possible input combinations; only 32 permitted (since 32 AND gates) in a typical PLA
  - 32 AND terms permitted → large fan-in for OR gates as well
    - This makes PLAs slower and slightly more expensive than some alternatives to be discussed shortly
  - 8 outputs → could have shared minterms, but not required
Programmable Array Logic (PAL)

- Used to implement circuits in SOP form
- The connections in the AND plane are programmable
- The connections in the OR plane are NOT programmable
Example Schematic of a PAL

\[ f_1 = x_1x_2x_3' + x_1'x_2x_3 \]
\[ f_2 = x_1'x_2' + x_1x_2x_3 \]
Comparing PALs and PLAs

- PALs have the same limitations as PLAs (small number of allowed AND terms)
- PALs are simpler to manufacture, cheaper, and faster (better performance)
- PALs also often have extra circuitry connected to the output of each OR gate
  - The OR gate plus this circuitry is called a macrocell
Macrocell

OR gate from PAL

back to AND plane

Clock

Flip-flop

Select

Enable

\( f \)
Macrocell Functions

- **Enable = 0**
  Allow the output pin for $f_1$ to be used as an additional input pin to the PAL

- **Enable = 1, Select = 0**
  Typical PAL operation

- **Enable = Select = 1**
  Allows the PAL to synchronize the output changes with a clock pulse

- The feedback to the AND plane provides multi-level design
Multi-Level Design with PALs

- \( f = A'BC + A'B'C' + ABC' + AB'C \)

where \( g = BC + B'C' \) and \( C = h \)
22V10 PAL

I/Clock = Input/Clock
I = Input
I/O = Input/Output

SP = Synchronous Reset
AC = Asynchronous Clear
OE = Output Enable
Complex Programmable Logic Devices

• What is the next step in the evolution of programmable logic?

  More gates!

• How do we get more gate?

  Put several PALs on one chip and put an interconnection matrix between them! → CPLD
Complex Programmable Logic Devices (CPLD)

- SPLDs (PLA, PAL) are limited in size due to the small number of input and output pins and the limited number of product terms
  - Combined number of inputs + outputs < 32 or so
- CPLDs contain multiple circuit blocks on a single chip
  - Each block is like a PAL: PAL-like block
  - Connections are provided between PAL-like blocks via an interconnection network that is programmable
  - Each block is connected to an I/O block as well
**CPLD Concept**

- Constructed of several interconnected PLDs (i.e. simple programmable logic devices) on a single chip
- Simplest CPLD chips, e.g. ispMACH 4032, are much more powerful than a 22V10
- Like PLDs, intended to replace discrete logic chips
- They bridge the gap between simple PLDs and very complex FPGA
- Software aids same as in PLD design:
  - ABEL, VHDL, SystemVerilog and underlying simulators such as Modelsim
  - Synplify for automated logic synthesis (nb. embedded in Lattice Diamond)
  - Lattice Diamond (or equivalent manufacturer’s tool, e.g. ispLever + Synplify) for design placement and routing
Structure of a CPLD

- PAL-like block
- I/O block
- Interconnection wires

Diagram showing the structure of a CPLD with interconnection wires between PAL-like blocks and I/O blocks.
Internal Structure of a PAL-like Block

- Includes macrocells
  - Usually about 16 each

- Fixed OR planes
  - OR gates have fan-in between 5-20

- XOR gates provide negation ability
  - XOR has a control input
More on PAL-like Blocks

- CPLD pins are provided to control XOR, MUX, and tri-state gates

- When tri-state gate is disabled, the corresponding output pin can be used as an input pin
  - The associated PAL-like block is then useless

- The AND plane and interconnection network are programmable

- Commercial CPLDs have between 2-100 PAL-like blocks
Programming a CPLD

• CPLDs have many pins – large ones have > 200
  • Removal of CPLD from a PCB is difficult without breaking the pins
  • Use ISP (in system programming) to program the CPLD
  • JTAG (Joint Test Action Group) port used to connect the CPLD to a computer
Example CPLD

- Use a CPLD to implement the function

\[ f = x_1 x_3 x_6' + x_1 x_4 x_5 x_6' + x_2 x_3 x_7 + x_2 x_4 x_5 x_7 \]

(from interconnection wires)
CPLD example – ispMACH from Lattice

ORP – Output routing pool
Generic Logic Block – equivalent of a simple PLD
Generic Logic Block

- Consists of a programmable AND array, logic allocator, 16 macrocells, and a GLB clock generator.
Macrocell
Output Routing Pool

- Allow macrocell outputs to be connected to any of several I/O cells within an I/O block
More advanced CPLD example – MACH XO from Lattice

- sysCLOCK PLLs
- Frequency Synthesis & Clock Alignment
- sysMEM Block RAM
- 9kbit Dual Port
- Flexible Routing
- Optimized for Speed, Cost and Routability
- sysIO Buffers Support
- LVCMOS/LVTTL, LVDS and PCI
- Programmable Function Units (PFUs)
- (with RAM)
- Programmable Function Units (PFFs)
- (without RAM)
- JTAG Port
sysIO Interfaces

- **sysIO Buffer Supports Multiple I/O Standards**
  - LVTTL, LVCMOS 33/25/18/15/12
  - PCI*
  - LVDS*, BLVDS**, LVPECL**
- **Up to 8 I/O Banks For Flexibility in I/O Placement**
- **Hotsocketing**
  - Input leakage less than 1mA during power-up/power-down
  - Power supplies can be sequenced in any order
- **Programmable Slew Rate**
- **Programmable Drive Strength**
  - 4 to 20mA (3.3-volts)
  - 4 to 20mA (2.5-volts)
  - 4 to 16mA (1.8-volts)
  - 4 to 8mA (1.5-volts)
  - 2 to 6mA (1.2-volts)
- **Programmable Pull-up, Pull-down, Bus-friendly**
  * MachXO 1200 and 2280
  ** MachXO 1200 and 2280 with external resistors
- **Programmable Open Drain**
sysMEM Block RAM

- Provides 9,216 Bit Blocks
- 275MHz Operation
- Efficient Implementation of Buffers

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<tr>
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<th>Single Port</th>
<th>Dual Port</th>
<th>Pseudo Dual Port</th>
<th>FIFO</th>
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<tbody>
<tr>
<td>RAM (Single Port)</td>
<td>8,192 X 1</td>
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<td>RAM (Dual Port)</td>
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<tr>
<td>RAM (Pseudo Dual Port)</td>
<td>256 X 36</td>
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- Configurable Width and Depth
- Single Port, Dual Port, Pseudo-Dual Port, FIFO and ROM Modes
- FIFO Logic Included in EBR
sysCLOCK PLL

- Frequency: 25MHz - 420 MHz
  - VCO Frequency 420-840 MHz
- Low Output Period Jitter: ~ +-120ps
- Programmable Phase / Duty Cycle (45 Degree Steps)
- Dynamic Delay Adjust
  - Increments of 250ps with a total of 2ns lead or 2ns lag
MACH XO programming and configuration

- On Chip FLASH
  Excellent Security

- Massively Parallel Wide Data Transfer Provides Fast SRAM Configuration from FLASH “Instant-on”

- Can configure SRAM Through JTAG

- Can reprogram FLASH Through JTAG Port
MachXO

SRAM
- Contains active configuration (define the circuit connection)
- Configure using ispJTAG
- Data stored in on-chip

Flash
- Provides internal storage for the configuration data
- Program using ispJTAG
- Direct mode (if SRAM is blank)
- Secure (Multiple security fuses to prevent unauthorized readback of the configuration data)

Instant-on at power up (Data rapidly loads from Flash memory to SRAM)